SPECIFICATIONS

# PXIe-5775

## PXI FlexRIO Digitizer

This document lists the specifications for the PXIe-5775. Specifications are subject to change without notice. For the most recent device specifications, refer to *ni.com/support*.

# Contents



# Definitions

*Warranted* specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

*Characteristics* describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

NATIONAL INSTRUMENTS

Specifications are *Typical* unless otherwise noted.

# Digital I/O

| | |
|---|---|
| Connector | Molex™ Nano-Pitch I/O™ |
| 5.0 V Power | ±5%, 50 mA maximum, nominal |

**Table 1.** Digital I/O Signal Characteristics

| Signal | Type | Direction |
|---|---|---|
| MGT Tx± <0..3>[1] | Xilinx UltraScale GTH | Output |
| MGT Rx± <0..3>[1] | Xilinx UltraScale GTH | Input |
| DIO <0..7> | Single-ended | Bidirectional |
| 5.0 V | DC | Output |
| GND | Ground | — |

# Digital I/O Single-Ended Channels

| | |
|---|---|
| Number of channels | 8 |
| Signal type | Single-ended |
| Voltage families | 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V |
| Input impedance | 100 kΩ, nominal |
| Output impedance | 50 Ω, nominal |
| Direction control | Per channel |
| Minimum required direction change latency | 200 ns |
| Maximum output toggle rate | 60 MHz with 100 µA load, nominal |

**Table 2.** Digital I/O Single-Ended DC Signal Characteristics[2]

| Voltage Family | $V_{IL}$ | $V_{IH}$ | $V_{OL}$ (100µA load) | $V_{OH}$ (100µA load) | Maximum DC Drive Strength |
|---|---|---|---|---|---|
| 3.3 V | 0.8 V | 2.0 V | 0.2 V | 3.0 V | 24 mA |
| 2.5 V | 0.7 V | 1.6 V | 0.2 V | 2.2 V | 18 mA |

[1] Multi-gigabit transceiver (MGT) signals are available on devices with KU040 and KU060 FPGAs only.

[2] Voltage levels are guaranteed by design through the digital buffer specifications.

**Table 2.** Digital I/O Single-Ended DC Signal Characteristics[2] (Continued)

| Voltage Family | $V_{IL}$ | $V_{IH}$ | $V_{OL}$ (100µA load) | $V_{OH}$ (100µA load) | Maximum DC Drive Strength |
|---|---|---|---|---|---|
| 1.8 V | 0.62 V | 1.29 V | 0.2 V | 1.5 V | 16 mA |
| 1.5 V | 0.51 V | 1.07 V | 0.2 V | 1.2 V | 12 mA |
| 1.2 V | 0.42 V | 0.87 V | 0.2 V | 0.9 V | 6 mA |

## Digital I/O High-Speed Serial MGT[3]

**Note** MGTs are available on devices with KU040 and KU060 FPGAs only.

| | |
|---|---|
| Data rate | 500 Mbps to 16.375 Gbps, nominal |
| Number of Tx channels | 4 |
| Number of Rx channels | 4 |
| I/O AC coupling capacitor | 100 nF |

### MGT TX± Channels

| | |
|---|---|
| Minimum differential output voltage[4] | 170 mV pk-pk into 100 Ω, nominal |
| I/O coupling | AC-coupled with 100 nF capacitor |

### MGT RX± Channels

| | |
|---|---|
| Differential input voltage range | |
| ≤ 6.6 Gb/s | 150 mV pk-pk to 2000 mV pk-pk, nominal |
| > 6.6 Gb/s | 150 mV pk-pk to 1250 mV pk-pk, nominal |
| Differential input resistance | 100 Ω, nominal |
| I/O coupling | DC-coupled, requires external capacitor ⚠ |

# Reconfigurable FPGA

PXIe-5775 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PXIe-5775 FPGA options.

[2] Voltage levels are guaranteed by design through the digital buffer specifications.
[3] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.
[4] 800 mV pk-pk when transmitter output swing is set to the maximum setting.

**Table 3.** Reconfigurable FPGA Options

| | KU035 | KU040 | KU060 |
|---|---|---|---|
| LUTs | 203,128 | 242,200 | 331,680 |
| DSP48 slices (25 × 18 multiplier) | 1,700 | 1,920 | 2,760 |
| Embedded Block RAM | 19.0 Mb | 21.1 Mb | 38.0 Mb |
| Data Clock Domain | 200 MHz, 16 samples per cycle per channel (dual channel mode), 32 samples per cycle (single channel mode) | | |
| Timebase reference sources | PXI Express 100 MHz (PXIe_CLK100) | | |
| Data transfers | DMA, interrupts, programmed I/O | DMA, interrupts, programmed I/O, multi-gigabit transceivers | |
| Number of DMA channels | 60 | | |

**Note** The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

# Onboard DRAM

**Note** DRAM is available on devices with KU040 and KU060 FPGAs only.

| | |
|---|---|
| Memory size | 4 GB (2 banks of 2 GB) |
| DRAM clock rate | 1064 MHz |
| Physical bus width | 32 bit |
| LabVIEW FPGA DRAM clock rate | 267 MHz |
| LabVIEW FPGA DRAM bus width | 256 bit per bank |
| Maximum theoretical data rate | 17 GB/s (8.5 GB/s per bank) |

# Analog Input

## General Characteristics

| | |
|---|---|
| Number of channels | 2, single-ended, simultaneously sampled |
| Connector type | SMA |
| Input impedance | 50 Ω |
| Input coupling | AC |
| Sample Clock | |
| Internal Sample Clock | 3.2 GHz |
| External Sample Clock | 2.8 GHz to 3.2 GHz |
| Sample Rate | |
| Dual channel mode | 3.2 GS/s per channel |
| Single channel mode | 6.4 GS/s |
| Analog-to-digital converter (ADC) | ADC12DJ3200, 12-bit resolution |
| Input latency[5] | 239 ns |

## Typical Specifications

| | |
|---|---|
| Full-scale input range | 1.25 V pk-pk (5.92 dBm) at 10 MHz |
| AC gain accuracy | ±0.11 dB at 10 MHz |
| DC offset | ±2.19 mV |
| Bandwidth (-3 dB)[6] | 500 kHz to 6 GHz |

**Table 4.** Single-Tone Spectral Performance, Dual Channel Mode

| | Input Frequency | | | | |
|---|---|---|---|---|---|
| | **99.9 MHz** | **399 MHz** | **999 MHz** | **1.999 GHz** | **2.499 GHz** |
| SNR[7] (dBFS) | 56.0 | 55.6 | 54.7 | 52.9 | 51.6 |
| SINAD[7] (dBFS) | 55.5 | 55.0 | 54.0 | 51.8 | 50.8 |
| SFDR (dBc) | -64.9 | -63.4 | -62.7 | -59.9 | -58.6 |
| ENOB[8] (bits) | 8.9 | 8.8 | 8.7 | 8.3 | 8.1 |

5 SMA input to LabVIEW diagram
6 Normalized to 10 MHz.
7 Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.
8 Calculated from SINAD and corrected to full scale.

**Table 5.** Single-Tone Spectral Performance, Single Channel Mode[9]

| | Input Frequency | | | | |
|---|---|---|---|---|---|
| | **99.9 MHz** | **399 MHz** | **999 MHz** | **1.999 GHz** | **2.499 GHz** |
| SNR[7] (dBFS) | 54.6 | 54.2 | 52.4 | 49.7 | 48.9 |
| SINAD[7] (dBFS) | 54.4 | 53.9 | 52.1 | 49.4 | 48.6 |
| SFDR (dBc) | -61.7 | -60.4 | -56.1 | -51.7 | -51.1 |
| ENOB[8] (bits) | 8.7 | 8.7 | 8.4 | 7.9 | 7.8 |

**Table 6.** Noise Spectral Density[10]

| **Mode** | $\frac{nV}{\sqrt{Hz}}$ | $\frac{dBm}{Hz}$ | $\frac{dBFS}{Hz}$ |
|---|---|---|---|
| Dual channel | 14.4 | -143.8 | -149.2 |
| Single channel | 9.8 | -147.2 | -152.6 |

**Note** Noise spectral density is verified using a 50 Ω terminator connected to the input.

[9] Measured using channel AI0. Spectral performance may be degraded using channel AI1.
[10] Excludes fixed interleaving spur (Fs/2 spur).

**Figure 1.** Single Tone Spectrum (Dual Channel Mode, 99.9 MHz, -1 dBFS, 3.2 kHz RBW), Measured

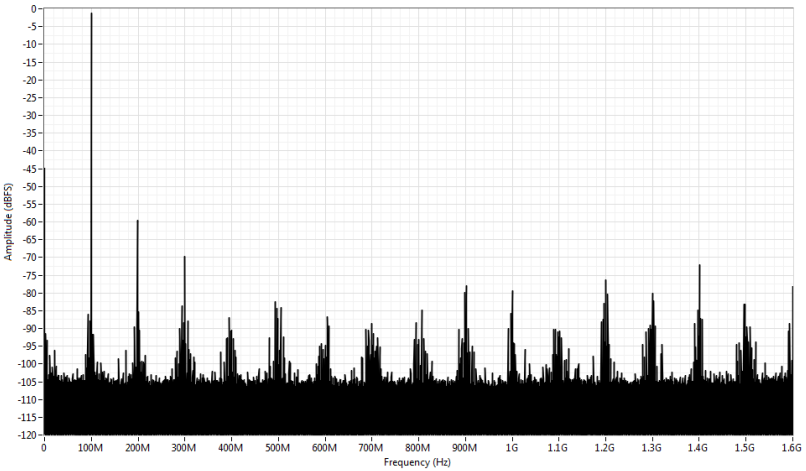



**Figure 2.** Single Tone Spectrum (Dual Channel Mode, 1.999 GHz, -1 dBFS, 3.2 kHz RBW), Measured

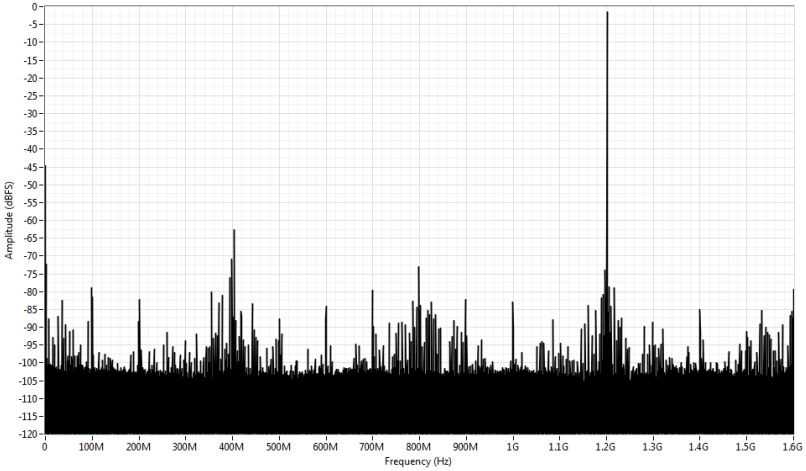


**Figure 3.** Single Tone Spectrum (Single Channel Mode, 99.9 MHz, -1 dBFS, 3.2 kHz RBW), Measured

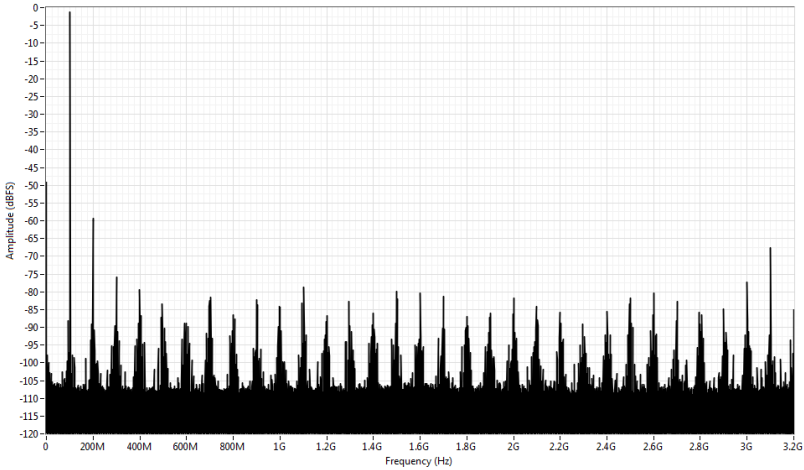
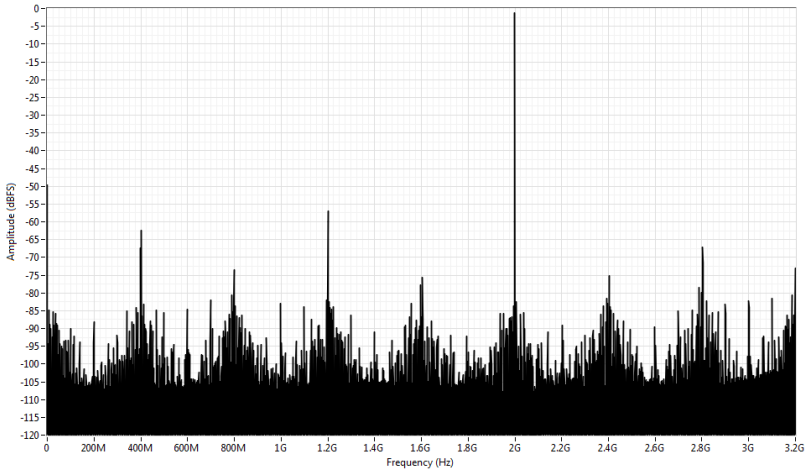



**Figure 4.** Single Tone Spectrum (Single Channel Mode, 1.999 GHz, -1 dBFS, 3.2 kHz RBW), Measured




| Channel-to-channel crosstalk, measured | |
|---|---|
| 99.9 MHz | -92.5 dB |
| 399 MHz | -85.5 dB |
| 999 MHz | -76.5 dB |

| | |
|---|---|
| 1.999 GHz | -68.8 dB |
| 2.499 GHz | -67.4 dB |

**Figure 5.** Analog Input Frequency Response, Measured

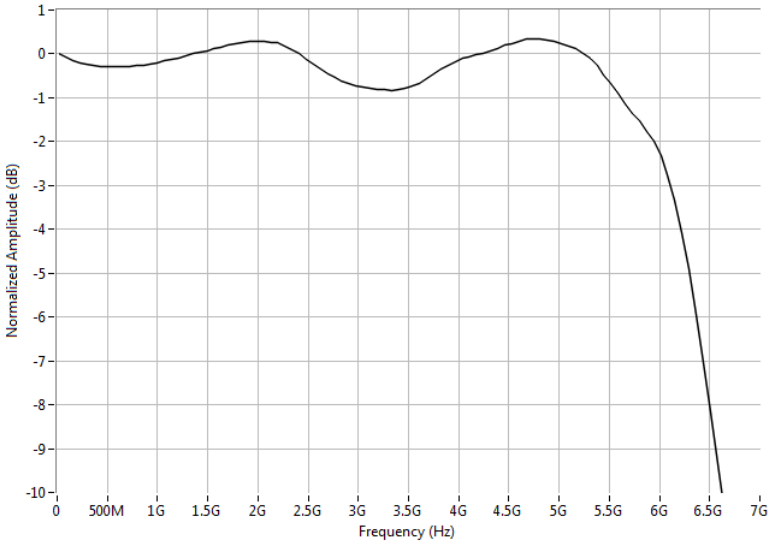
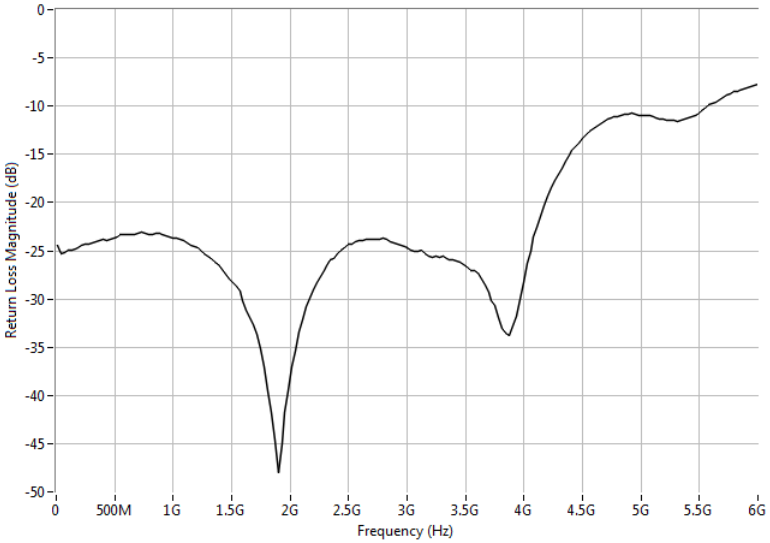


**Figure 6.** Input Return Loss, Measured




# CLK/REF IN

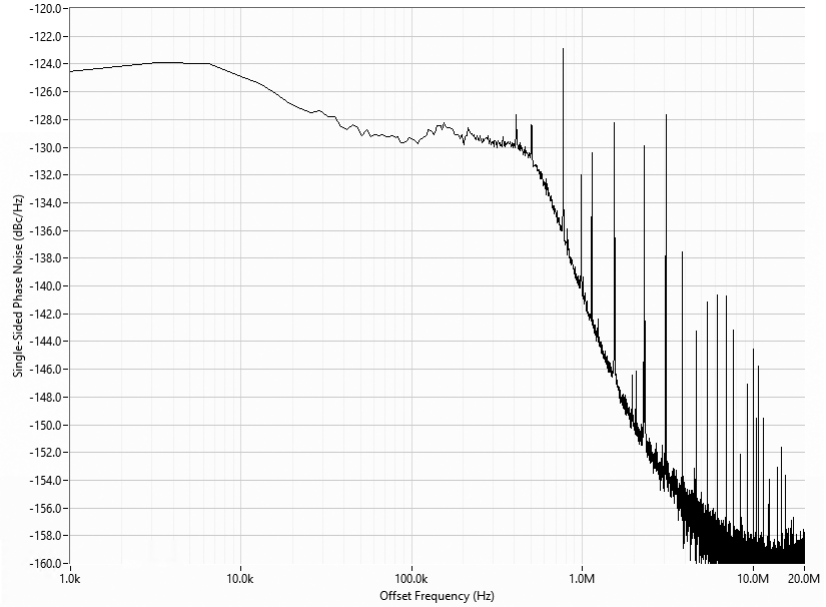
| | |
|---|---|
| Connector type | SMA |
| Input impedance | 50 Ω |
| Input coupling | AC |
| Input voltage range | 0.35 V pk-pk to 3.5 V pk-pk |
| Absolute maximum voltage | ±12 V DC, 4 V pk-pk AC |
| Duty cycle | 45% to 55% |
| Sample Clock jitter[11] | 86.8 fs RMS, measured |

[11] Integrated from 3.2 kHz to 20 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

**Table 7.** Clock Configuration Options

| Clock Configuration | External Clock Frequency | Description |
|---|---|---|
| Internal PXI_CLK10[12] | 10 MHz | The internal Sample Clock locks to the PXI 10 MHz Reference Clock, which is provided through the backplane. |
| External Reference Clock (CLK/REF IN) | 10 MHz[13] | The internal Sample Clock locks to an external Reference Clock, which is provided through the CLK/REF IN front panel connector. |
| External Sample Clock (CLK/REF IN) | 2.0 GHz to 3.2 GHz | An external Sample Clock can be provided through the CLK/REF IN front panel connector. |

**Figure 7.** Phase Noise with 800 MHz Input Tone, Measured




12 Default clock configuration.
13 The external Reference Clock must be accurate to ±25 ppm.

# Bus Interface

| | |
|---|---|
| Form factor | PCI Express Gen-3 x8 |

# Maximum Power Requirements

**Note** Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

| | |
|---|---|
| +3.3 V | 3 A |
| +12 V | 4 A |
| Maximum total power | 58 W |

# Physical

| | |
|---|---|
| Dimensions (not including connectors) | 18.8 cm × 12.9 cm (7.4 in. × 5.1 in.) |
| Weight | 190 g (6.7 oz) |

# Environment

| | |
|---|---|
| Maximum altitude | 2,000 m (800 mbar) (at 25 °C ambient temperature) |
| Pollution Degree | 2 |

Indoor use only.

## Operating Environment

| | |
|---|---|
| Ambient temperature range | 0 °C to 55 °C[14] (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.) |
| Relative humidity range | 10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.) |

[14] The PXIe-5775 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the *PXI Chassis Manual* for specifications to determine the ambient temperature ranges your chassis can achieve.

## Storage Environment

| | |
|---|---|
| Ambient temperature range | -40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 4 limits.) |
| Relative humidity range | 5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.) |

# Shock and Vibration

| | |
|---|---|
| Operating shock | 30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.) |
| Random vibration | |
| Operating | 5 Hz to 500 Hz, 0.3 $g_{rms}$ (Tested in accordance with IEC 60068-2-64.) |
| Nonoperating | 5 Hz to 500 Hz, 2.4 $g_{rms}$ (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.) |

# TCLK Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample Clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help* within the *FlexRIO Help*. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

## Intermodule Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample Clocks of each module.

- All parameters are set to identical values for each module.
- Modules are synchronized without using an external Sample Clock.

**Note** Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

| | |
|---|---|
| Skew[15] | 80 ps, measured |
| Skew after manual adjustment | ≤10 ps, measured |
| Sample Clock delay/adjustment | 0.4 ps |

[15] Caused by clock and analog delay differences. No manual adjustment performed. Tested with a PXIe-1085 chassis with a 24 GB backplane with a maximum slot to slot skew of 100 ps. Measured at 23 °C.